REMARKS

Claims 1-5 and 7-24 remain pending in the current Application. Claim 1 has been amended; and claims 6 and 25-28 (non-elected claims) have been cancelled. Applicant submits that the amendments do not add new matter to the current Application. All the amendments herein have been made in order to clarify the claims and not for prior art reasons. Applicant also submits that (1) no amendment made was related to the statutory requirements of patentability unless expressly stated herein, and (2) no amendment made was for the purpose of narrowing the scope of any claim, unless Applicant has argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Specification

The Examiner requests a new more descriptive title. Therefore, Applicants are changing the title to "METHOD FOR FORMING MULTIPLE GATE OXIDE THICKNESSES UTILIZING ASHING AND CLEANING." Note that Applicants are using "multiple gate oxide thicknesses" rather than "dual gate oxide thickness," as suggested by the Examiner, because the current application and claims may be used to form more than two different gate oxide thicknesses.

Drawings

The Examiner states that an SOI substrate, as recited in claim 2, is not illustrated in the drawings. However, Applicant disagrees. For example, referring to FIGs. 1-5, and the text accompanying FIG. 1, substrate 12 is clearly described as being either a bulk substrate or an SOI substrate (See pg. 6, lines 11-12, of the current Application). Therefore, FIGs. 1-5 illustrate an SOI substrate as well as a bulk substrate or any other type of substrate as described in the application in reference to substrate 12.

The Examiner also states that the triple gate oxide (TGO) process as recited in claim 23 is not shown. However, referring to FIG. 7, block 80, a TGO process is clearly illustrated where block 80 states "repeat 70 to 80 if more gate dielectric regions are desired (e.g. for triple gate

oxide (TGO) processes)." Therefore, the processing described in reference to blocks 66 to 78 of FIG. 7 and the processing illustrated with respect to FIGs. 1-5 also illustrate a TGO process.

Rejection of claims 1-24 under 35 U.S.C. 112

Applicants submit that claim 1, reciting "ashing the portion of remaining dielectric layer within the region ..." is clear and definite. Although it is known in the art that "ashing" is a plasma process that may be used to remove photoresist, the current Application uses ashing to actually affect the dielectric layer by increasing its thickness. That is, ashing, a known process, is being used in a different way to affect something other than or in addition to photoresist. The specification clearly describes how ashing is used to affect dielectric layer 20 (see, e.g., FIGs. 2 and 3). That is, as described throughout the specification, one of the primary reasons for ashing in the current application is to expose the portion of the remaining dielectric layer (e.g. layer 20 of FIG. 2) to an ashing process (e.g. an oxygen plasma) in order to increase the overall thickness (e.g. by forming layer 22, thus increasing overall thickness of layer 20 as seen in FIG. 3) and not just to remove photoresist. Therefore, for at least these reasons, Applicants submit that the language of claim 1 is clear and therefore patentable under 35 U.S.C. 112.

Rejection of claims 1-14 and 18-24 under 35 U.S.C. 103(a)

Applicant respectfully submits that claims 1-14 and 18-24 are patentable over US Pub. No. 2003/0157772 (hereinafter referred to as Wieczorek) and US Patent No. 5,631,178 (hereinafter referred to as Vogel). Referring to claim 1, Applicants submit that Wieczorek nor Vogel, alone or in combination, teach or suggest ashing to increase a thickness of the dielectric layer, as claimed in claim 1. With respect to Wieczorek, Wieczorek speaks only to removing photoresist (paragraph 49) but does not specify how to remove the photoresist. The Examiner further states that Vogel describes ashing to remove photoresist. However, there is no motivation to use ashing for removing photoresist in Wieczorek. Firstly, ashing is not always necessary for removing photoresist, and in many cases is not used because the ashing process results in an increased processing time (and thus increases processing cost) as compared to other methods for removing photoresist. For example, ashing is typically used after doping where the

photoresist is hardened after implant. In this case, ashing (with its increased processing time) is necessary to properly remove the photoresist. However, in the step of Wieczorek where photoresist is removed, other processes other than ashing would be used because ashing would unnecessarily increase time and cost. That is, since ashing is not necessary at this step, one of ordinary skill in the art would not be motivated to do so because one of ordinary skill in the art would not be motivated to increase processing costs unnecessarily.

Also, neither Wieczorek nor Vogel even discuss increasing a thickness of a dielectric layer by ashing, as claimed in claim 1. Furthermore, note that Applicants have clarified claim 1 by specifying that the first intermediate thickness, after etching and prior to ashing is less than approximately 10 Angstroms, and that the second intermediate thickness, after ashing, is in a range of approximately 15 to 20 Angstroms. That is, even though Wieczorek describes a final oxide thickness of being in a range of tenths of nanometers (paragraph 57), Wieczorek does not teach or suggest any specific intermediate thicknesses. Also, even if an ashing process is unnecessarily performed in Wieczorek, the ashing process may still not result in an increased thickness of the dielectric layer or an adequate thickness of the dielectric layer. That is, Wieczorek makes no mention of increasing a thickness to approximately 15 to 20 Angstroms by ashing and, furthermore, makes no mention of then decreasing this thickness by a subsequent cleaning, prior to thermally oxidizing to reach the target thickness. These intermediate changes in thicknesses are not taught or suggested by Wieczorek and Vogel, alone or in combination, and one would not be motivated to do so, since extra processing steps would be added. Therefore, for at least these reasons, Applicants submit that claim 1 is patentable over Wieczorek in view of Vogel.

Claims 2-5 and 7-24 have not been independently addressed because they depend directly or indirectly from allowable claim 1, and are therefore allowable for at least those reasons stated above with respect to claim 1.

Conclusion

Although Applicants may disagree with statements made by the Examiner in reference to the claims and the cited references, Applicants are not discussing all these statements in the current Office Action, yet reserve the right to address them at a later time if necessary.

Applicants respectfully solicit allowance of the pending claims. Contact me if there are any issues regarding this communication or the current Application.

Respectfully submitted,

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